new abstract, replaced the original specification with a substitute specification, and amended claims 1, 5, and 8-10.

However, the Office Action of October 4, 2000, does not acknowledge the preliminary amendment of March 8, 1999. Accordingly, it is respectfully indicated that the Examiner specifically indicate on the record in the next Office communication (1) whether the preliminary amendment of March 8, 1999, has been entered, and (2) whether the substitute specification submitted with the preliminary amendment of March 8, 1999, has been entered.

The Office Action of October 4, 2000, includes a form PTO-892 on which the name of U.S. Patent No. 5,973,660 is misspelled as Hahimoto. The correct spelling is Hashimoto. Accordingly, it is respectfully requested that the Examiner provide a corrected form PTO-892 showing the correct spelling of Hashimoto with the next Office communication.

On page 2 of the Office Action of October 4, 2000, the Examiner states as follows in pertinent part:

> Claims 1-12 and in particular 9 are directed to the same invention as that of claim 19 of commonly assigned allowed application, U.S. Serial Number 09/450,436. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.
>
> Since the Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis

> for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.
>
> Failure to comply with this requirement will result in a holding of abandonment of this application.

U.S. patent application Serial No. 09/450,436 referred to by the Examiner issued as U.S. Patent No. 6,166,725 on December 26, 2000. Claim 19 of U.S. patent application Serial No. 09/450,436 is now claim 1 (the only claim) of U.S. Patent No. 6,166,725.

The Examiner's requirement that the common assignees (there are two) of U.S. Patent No. 6,166,725 and the present application state which inventive entity is the prior inventor of the conflicting subject matter identified by the Examiner has presumably been made pursuant to 37 CFR 1.78(c) and MPEP 804.03.

MPEP 804.03 (Seventh Edition, July 1998) provides as follows in pertinent part (emphasis by underlining added):

> Form Paragraphs 8.27, 8.28, and 8.28.01 may be used to require the applicant to name the prior inventor under 37 CFR 1.78(c).
>
> Before making the requirement to state the prior inventor under 37 CFR 1.78(c), with its threat to hold the case abandoned if the statement is not made by the assignee, <u>the examiner must make sure that claims are present in each case which are conflicting as defined in MPEP § 804</u>. See *In re Rekers*, 203 USPQ 1034 (Comm'r Pat. 1979).
>
> . . . .
>
> ¶ 8.27 *Different Inventors, Common Assignee, Same Invention*

> Claim[1] directed to the same invention as that of claim[2] of commonly assigned [3]. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.
>
> Since the Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.
>
> Failure to comply with this requirement will result in a holding of abandonment of this application.
>
> **Examiner Note:**
>
> 1. In bracket 3, insert the U.S. patent number or the copending application number.
>
> 2. The claims listed in brackets 1 and 2 must be for the same invention. If one invention is obvious in view of the other, do not use this paragraph; see form paragraph 8.28.
>
> 3. A provisional or actual statutory double patenting rejection may also be made using form paragraphs 8.31 or 8.32.
>
> 4. If the commonly assigned application or patent has an earlier U.S. filing date, a rejection under 35 U.S.C. 102(e) may also be made using form paragraph 7.15.01 or 7.15.02.

Thus, it appears from this passage of MPEP 804.03 that the Examiner is of the opinion that claims 1-12 of the present application and claim 19 of U.S. patent application Serial No.

09/450,436 (now claim 1 of U.S. Patent No. 6,166,725) claim the same invention.

MPEP 804 (Seventh Edition, July 1998) referred to in the above passage of MPEP 804.03 provides as follows in pertinent part (emphasis by underlining added):

> **A.** ***Statutory Double Patenting--35 U.S.C. 101***
>
> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. (Citations omitted.)

Independent claims 1, 5, and 9 of the present application (the only independent claims of the application) read as follows (emphasis added):

> 1. A liquid crystal display device comprising:
>
> a liquid crystal display panel; and
>
> a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; said picture signal line driving circuit having a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, and a second transistor, to whose gate electrode a bias voltage is applied, are connected in series.
>
> 5. A liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; said picture signal line driving circuit further including:

a first input terminal, a second input terminal, and a common output terminal,

a first switching element connected between the first input terminal and the common output terminal, and

a second switching element connected between the second input terminal and the common output terminal,

the first and second switching elements including a transistor at an input port, to whose gate electrode a control voltage is applied, connected in series with a transistor at an output port, to whose gate electrode a bias voltage is applied.

9. A liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; the picture signal line driving circuit further comprising:

a first output circuit for outputting a positive-polarity picture signal voltage,

a second output circuit for outputting a negative-polarity picture signal voltage, and

a switching circuit for switching the positive-polarity picture signal voltage supplied from the first output circuit and the negative-polarity picture signal voltage supplied from the second output circuit to a pair of picture signal lines and outputting the voltages, the switching circuit further including:

a first switching element connected between the first output circuit and the first picture signal line of the picture signal line pair,

a third switching element connected between the first output circuit and the

second picture signal line of the picture signal line pair,

a second switching element connected between the second output circuit and the second picture signal line, and

a fourth switching element connected between the second output circuit and the first picture signal line,

wherein a positive-polarity picture signal voltage supplied from the first output circuit is output to the first or second picture signal line by selectively turning on/off the first, second, third, and fourth switching elements,

a negative-polarity picture signal voltage supplied from the second output circuit is output to the second or first picture signal line by selectively turning on/off the first, second, third, and fourth switching elements,

and the switching elements are constituted by connecting a transistor at an output circuit side to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose gate electrode a constant bias voltage is applied.

Claim 1 of U.S. Patent No. 6,166,725 (the only claim of the patent) (corresponding to claim 19 of U.S. patent application Serial No. 09/450,436 referred to by the Examiner) reads as follows:

1. A liquid crystal display device comprising

a liquid crystal display panel including

a plurality of video signal lines,

a plurality of scanning signal lines perpendicular to the plurality of video signal lines, and

a plurality of pixels arranged in a matrix and each surrounded by two adjacent video signal lines among the plurality of video signal lines and by two adjacent scanning signal lines among the plurality of scanning signal lines;

a video signal line drive circuit connected to each of the plurality of video signal lines which outputs LC driving voltages to each of the plurality of video signal lines to apply the LC driving voltages to each of the plurality of pixels; and

a display control circuit which controls and drives the video signal line drive circuit;

wherein the video signal line drive circuit includes:

a first drive voltage circuit including

at least one first output circuit each including a latch circuit which latches display data, and a decoder circuit which selects and outputs an LC driving voltage of positive polarity corresponding to the display data, and

at least one second output circuit each including a latch circuit which latches display data, and a decoder circuit which selects and outputs an LC driving voltage of negative polarity corresponding to the display data,

the at least one first output circuit and the at least one second output circuit being arranged alternately in a first polarity order;

a second drive voltage circuit including

at least one third output circuit each including a latch circuit which latches display data, and a decoder circuit which selects and outputs an LC driving voltage of positive polarity corresponding to the display data, and

at least one fourth output circuit each including a latch circuit which latches display data, and a decoder circuit which selects and outputs an LC driving voltage of negative polarity corresponding to the display data,

the at least one third output circuit and the at least one fourth output circuit being arranged alternately in a second polarity order opposite to the first polarity order in which the at least one first output circuit and the at least one second output circuit of the first drive voltage circuit are arranged alternately;

a first switching circuit which inputs display data sequentially transferred from the display control circuit to the latch circuits of the first voltage drive circuit and the second voltage drive circuit in

a first input order in which display data is sequentially inputted first to the latch circuits of the first drive voltage circuit and then to the latch circuits of the second drive voltage circuit, and

a second input order in which display data is sequentially inputted first to the latch circuits of the second drive voltage circuit and then to the latch circuits of the first drive voltage circuit,

the first switching circuit alternating the first input order and the second input order based on a display control signal from the display control circuit; and

a second switching circuit which supplies outputs from the first drive voltage circuit and the second drive voltage circuit to each of the plurality of video signal lines in

a first output arrangement corresponding to the first input order of the first switching circuit, and

a second output arrangement corresponding to the second input order of the first switching circuit,

the second switching circuit alternating the first output arrangement and the second output arrangement in synchronism with the alternation of the first input order and the second input order by the first switching circuit.

It is submitted that it is readily apparent from a comparison of application claims 1, 5, and 9 and patent claim 1 that patent claim 1 does not recite a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, and a second transistor, to whose gate electrode a bias voltage is applied, are connected in series as recited in application claim 1; that patent claim 1 does not recite first and second switching elements including a transistor at an input port, to whose gate electrode a control voltage is applied, connected in series with a transistor at an output port, to whose gate electrode a bias voltage is

applied as recited in application claim 5; and that patent claim 1 does not recite first, second, third, and fourth switching elements which are constituted by connecting a transistor at an output circuit side to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose gate electrode a constant bias voltage is applied as recited in application claim 9.

Since patent claim 1 does not recite certain features of independent application claims 1, 5, and 9 as discussed above, it is submitted that independent application claims 1, 5, and 9 and dependent applications claims 2-4, 6-8, and 10-12 depending therefrom (i.e. application claims 1-12) do not claim the same invention, i.e. identical subject matter, as patent claim 1. Accordingly, it is submitted that the Examiner cannot reject application claims 1-12 under 35 USC 101 as claiming the same invention as patent claim 1.

In light of this, it is submitted that the Examiner's requirement that the common assignees of U.S. Patent No. 6,166,725 and the present application state which inventive entity is the prior inventor of the alleged conflicting subject matter identified by the Examiner is improper because there is in fact no conflicting subject matter between application claims 1-12 and patent claim 1 for the reasons discussed above. Accordingly, it is respectfully requested that the Examiner's requirement be withdrawn.

Claims 1-8 were rejected under 35 USC 102(a) as being anticipated by Hashimoto. This rejection is respectfully traversed.

Independent claim 1 recites a liquid crystal display device comprising a liquid crystal display panel, and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, said picture signal line driving circuit having a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, and a second transistor, to whose gate electrode a bias voltage is applied, are connected in series.

Claim 2 recites the liquid crystal display device according to claim 1, wherein a first bias voltage is applied to the gate electrode of the second transistor and a second bias voltage is applied to a well layer provided with the first and the second transistors.

Claim 3 recites the liquid crystal display device according to claim 1, wherein the first and the second transistors are first conducting-type transistors, and a second conducting-type transistor is connected to the first transistor in parallel.

Claim 4 recites the liquid crystal display device according to claim 1, wherein the potential of the input terminal of the first transistor is equal to the potential applied to the well layer provided with the first and the second transistors.

In explaining the rejection of claims 1-4, the Examiner states as follows:

> **As in claim 1, Hashimoto teaches of** a liquid crystal display device comprising: a liquid crystal display panel, **column 1 lines 5-7**; and for supplying a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, **column 2 lines 5-42**; said picture signal line driving circuit having a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied and a second transistor to whose gate electrode a bias voltage is applied are connected in series, **figure 2**. As in claims **2, 3, and 4**, Hashimoto also teaches of said features, [column] 4 lines 1-50, and figure 2, wherein said features are illustrated in figure 2.

However, it is submitted that Fig. 2 of Hashimoto does not disclose a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, and a second transistor, to whose gate electrode a bias voltage is applied, are connected in series as recited in claim 1 as alleged by the Examiner. Nor is it seen where any other portion of Hashimoto discloses these features of claim 1.

Fig. 2 of Hashimoto shows switch circuits 4 and 8, but does not show any transistors. Figs. 8-11 of Hashimoto show transistors, but these transistors are part of low-voltage level shift circuit 10, high-voltage level shift circuit 9, high-voltage operational amplifier 13, and low-voltage operational amplifier 14 in Fig. 2, rather than part of switch circuits 4 and 8 in Fig. 2. Furthermore, the words "bias" and "series" do not appear anywhere in Hashimoto.

Accordingly, it is submitted that Hashimoto does not disclose a switching circuit in which a first transistor, to whose gate electrode a control voltage is applied, and a second transistor, to whose gate electrode a bias voltage is applied, are connected in series as recited in claim 1 as alleged by the Examiner.

Furthermore, it is submitted that column 4, lines 1-50, and Fig. 2 of Hashimoto do not discloses the features of claim 2 wherein a first bias voltage is applied to the gate electrode of the second transistor and a second bias voltage is applied to a well layer provided with the first and the second transistors; the features of claim 3 wherein the first and the second transistors are first conducting-type transistors, and a second conducting-type transistor is connected to the first transistor in parallel; or the features of claim 4 wherein the potential of the input terminal of the first transistor is equal to the potential applied to the well layer provided with the first and the second transistors as alleged by the Examiner. Nor is it seen where any other portion of Hashimoto discloses these features of claims 2-4, it being noted that the word "well" does not appear anywhere in Hashimoto.

Independent claim 5 recites a liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; said picture signal line driving circuit further including a first

input terminal, a second input terminal, and a common output terminal, a first switching element connected between the first input terminal and the common output terminal, and a second switching element connected between the second input terminal and the common output terminal, the first and second switching elements including a transistor at an input port, to whose gate electrode a control voltage is applied, connected in series with a transistor at an output port, to whose gate electrode a bias voltage is applied.

Claim 6 recites the liquid crystal display device according to claim 5, wherein the bias voltage applied to the gate electrode of the transistor at the input port is different from the bias voltage applied to a well layer provided with the transistor at the input port and the transistor at the output port.

Claim 7 recites the liquid crystal display device according to claim 5, wherein the transistor at the input port and the transistor at the output port of the first switching element are first conducting-type transistors, the transistor at the input port and the transistor at the output port of the second switching element are second conducting-type transistors, and the second conducting-type transistor is connected to the transistor at the input port of the first switching element in parallel and the first conducting-type transistor is connected to the transistor at the input port of the second switching element in parallel.

Claim 8 recites the liquid crystal display device according to claim 5, wherein the potential of the input terminal of the transistor at the input port is applied to the well layer provided with the transistor at the output port.

In explaining the rejection of claims 5-8, the Examiner states as follows:

> **As in claim 5, Hashimoto teaches of** a liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, **column 1 lines 5-7;** said picture signal line driving circuit further including: a first output terminal, a second input terminal, and a common output terminal, a first switching element connected between the first input terminal and the common output terminal, and a second switching element connected between the second input terminal and the common output terminal, the first and second switching elements including a transistor at a input port, to whose gate electrode a control voltage is applied connected in series with a transistor at a output port, to whose gate electrode a bias voltage is applied, column 2 lines 5-47, figure 2, 3, and 15 . As in **claims 6 and 7**, Hashimot teaches of said features, figure 3, column 4 lines 1-60, wherein said features are illustrated in figures 2 and 3.

However, it is submitted that column 2, lines 5-47, and Figs. 2-3 and 15 of Hashimoto do not disclose first and second switching elements including a transistor at an input port, to whose gate electrode a control voltage is applied, connected in series with a transistor at an output port, to whose gate electrode a bias voltage is applied as recited in claim 5 as alleged by the Examiner. Nor is it seen where any other portion of Hashimoto discloses these features of claim 5.

Fig. 2 of Hashimoto shows switch circuits 4 and 8, but does not show any transistors. Figs. 8-11 of Hashimoto show transistors, but these transistors are part of low-voltage level shift circuit 10, high-voltage level shift circuit 9, high-voltage operational amplifier 13, and low-voltage operational amplifier 14 in Fig. 2, rather than part of switch circuits 4 and 8 in Fig. 2. Furthermore, the words "series" and "bias" do not appear anywhere in Hashimoto.

Accordingly, it is submitted that Hashimoto does not disclose first and second switching elements including a transistor at an input port, to whose gate electrode a control voltage is applied, connected in series with a transistor at an output port, to whose gate electrode a bias voltage is applied as recited in claim 5 as alleged by the Examiner.

Furthermore, it is submitted that column 4, lines 1-60, and Figs. 2-3 of Hashimoto do not disclose the features of claim 6 wherein the bias voltage applied to the gate electrode of the transistor at the input port is different from the bias voltage applied to a well layer provided with the transistor at the input port and the transistor at the output port; or the features of claim 7 wherein the transistor at the input port and the transistor at the output port of the first switching element are first conducting-type transistors, the transistor at the input port and the transistor at the output port of the second switching element are second conducting-type transistors, and the second conducting-type transistor is connected to the transistor at the input port of

the first switching element in parallel and the first conducting-type transistor is connected to the transistor at the input port of the second switching element in parallel as alleged by the Examiner.

Furthermore, it is submitted that Hashimoto does not disclose the features of claim 8 wherein the potential of the input terminal of the transistor at the input port is applied to the well layer provided with the transistor at the output port, it being noted that the Examiner did not specifically mention claim 8 in the explanation of the rejection of claims 1-8 under 35 USC 102(a) as being anticipated by Hashimoto.

Nor is it seen where any other portion of Hashimoto discloses the features of claims 6-8 set forth above, it being noted that the word "well" does not appear anywhere in Hashimoto.

Since Hashimoto does not disclose the features of claims 1-8 discussed above, it is submitted that claims 1-8 patentably distinguish over Hashimoto in the sense of 35 USC 102(a), and it is respectfully requested that the rejection of claims 1-8 under 35 USC 102(a) as being anticipated by Hashimoto be withdrawn.

Claims 9-12 were rejected under 35 USC 102(a) as being anticipated by Kitamura. This rejection is respectfully traversed.

Independent claim 9 recites a liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture

signal voltage to the liquid crystal display panel; the picture signal line driving circuit further comprising a first output circuit for outputting a positive-polarity picture signal voltage, a second output circuit for outputting a negative-polarity picture signal voltage, and a switching circuit for switching the positive-polarity picture signal voltage supplied from the first output circuit and the negative-polarity picture signal voltage supplied from the second output circuit to a pair of picture signal lines and outputting the voltages, the switching circuit further including a first switching element connected between the first output circuit and the first picture signal line of the picture signal line pair, a third switching element connected between the first output circuit and the second picture signal line of the picture signal line pair, a second switching element connected between the second output circuit and the second picture signal line, and a fourth switching element connected between the second output circuit and the first picture signal line, wherein a positive-polarity picture signal voltage supplied from the first output circuit is output to the first or second picture signal line by selectively turning on/off the first, second, third, and fourth switching elements, a negative-polarity picture signal voltage supplied from the second output circuit is output to the second or first picture signal line by selectively turning on/off the first, second, third, and fourth switching elements, and the switching elements are constituted by

connecting a transistor at an output circuit side to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose gate electrode a constant bias voltage is applied.

Claim 10 recites the liquid crystal display device according to claim 9, wherein the bias voltage applied to the gate electrode of the transistor at the picture signal side is different from the bias voltage applied to a well layer provided with a transistor at an output port and a transistor at a picture signal side.

Claim 11 recites the liquid crystal display device according to claim 9, wherein the transistors at the output side and the picture signal side of the first and third switching elements are first conducting-type transistors and the transistors at the output port and the picture signal side of the second and fourth switching elements are second conducting-type transistors, and the second conducting-type transistors are connected in parallel with the transistors at the output port of the first and third switching elements and the first conducting-type transistors are connected in parallel with the transistors at the output port of the second and fourth switching elements.

Claim 12 recites the liquid crystal display device according to claim 9, wherein the potential of the input terminal of the transistor at the output circuit side is equal to the potential applied to the well layer provided with the transistor at the picture signal line side.

In explaining the rejection of claims 9-12, the Examiner states as follows:

> **As in claim 9, Kitamura teaches of** a liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, **column 1 lines 5-13**; the picture signal line driving circuit further comprising: a first output circuit for outputting a positive polarity picture signal voltage, a second output circuit for outputting a negative polarity picture signal voltage, and a switching circuit for switching the positive polarity picture signal voltage supplied from the first output circuit and the negative polarity picture signal voltage supplied from the second output circuit to a pair of picture signal lines and outputting the voltages, **column 2 lines 20-43**, the switching circuit further including: a first switching element connected between the first output circuit arid the first picture signal line of the picture signal line pair, a third switching element connected between the first output circuit and the second picture signal line of the picture signal line pair, a second switching element connected between the second output circuit and the second picture signal line, and a fourth switching element connected between the second output circuit and the first picture signal line, wherein a positive-polarity picture signal voltage supplied from the first output circuit is output to the first or second picture signal line by selectively turning on/off the first, second, third, and fourth switching elements, a negative-polarity picture signal voltage supplied from the second output circuit is output to the second or first picture signal line by selectively turning on/off the first, second, third, and fourth switching elements, and the switching elements are constituted by connecting a transistor at an output circuit to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose, gate

> electrode a constant bias voltage is applied, column 4 lines 24-76, column 5 lines 1-11, and figure 5. As in **claims 10, 11, and 12**, Kitamura also teaches of said features, column 2 lines 20-43, figures 4 and 5.

However, it is submitted that column 4, lines 24-76, column 5, lines 1-11, and Fig. 5 of Kitamura do not disclose first, second, third, and fourth switching elements which are constituted by connecting a transistor at an output circuit side to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose gate electrode a constant bias voltage is applied as recited in claim 9 as alleged by the Examiner. Nor is it seen where any other portion of Kitamura discloses these features of claim 9.

Fig. 5 of Kitamura shows switch circuits SWA_1 to SWA_n and SWB_1 to SWB_n each of which consists of a p-channel MOS transistor and an n-channel MOS transistor connected in parallel to each other as shown in Fig. 9 of Kitamura and described in column 3, lines 34-40, of Kitamura. However, it is submitted that Kitamura does not disclose that switch circuits SWA_1 to SWA_n and SWB_1 to SWB_n in Fig. 5 of Kitamura are constituted by connecting a transistor at an output circuit side to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose gate electrode a constant bias voltage is applied as recited in claim 9 of Kitamura. Furthermore, the words "series" and "bias" do not appear anywhere in Kitamura.

Accordingly, it is submitted that Kitamura does not disclose first, second, third, and fourth switching elements which are constituted by connecting a transistor at an output circuit side to whose gate electrode a control voltage is applied in series with a transistor at a picture signal line side to whose gate electrode a constant bias voltage is applied as recited in claim 9 as alleged by the Examiner.

Furthermore, it is submitted that column 2, lines 20-43, and Figs. 4-5 of Kitamura do not disclose or suggest the features of claim 10 wherein the bias voltage applied to the gate electrode of the transistor at the picture signal side is different from the bias voltage applied to a well layer provided with a transistor at an output port and a transistor at a picture signal side; the features of claim 11 wherein the transistors at the output side and the picture signal side of the first and third switching elements are first conducting-type transistors and the transistors at the output port and the picture signal side of the second and fourth switching elements are second conducting-type transistors, and the second conducting-type transistors are connected in parallel with the transistors at the output port of the first and third switching elements and the first conducting-type transistors are connected in parallel with the transistors at the output port of the second and fourth switching elements; or the features of claim 12 wherein the potential of the input terminal of the transistor at the output circuit side is equal to the potential applied to the well layer provided with the

transistor at the picture signal line side as alleged by the Examiner. Nor is it seen where any other portion of Kitamura discloses these features of claims 10-12, it being noted that the words "bias" and "well" do not appear anywhere in Kitamura.

Since Kitamura does not disclose the features of claims 9-12 discussed above, it is submitted that claims 9-12 patentably distinguish over Kitamura in the sense of 35 USC 102(a), and it is respectfully requested that the rejection of claims 9-12 under 35 USC 102(a) as being anticipated by Kitamura be withdrawn.

As recognized by the Examiner, the other references cited but not relied upon neither disclose nor suggest the present invention, and thus no further discussion of these other references is deemed necessary at this time.

It is submitted that all of the Examiner's rejections have been overcome, and that the application is now in condition for allowance. Reconsideration of the application and an action of a favorable nature are respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any

overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (501.36642X00).

Respectfully submitted,

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